REMARKS

Applicant respectfully requests the Examiner's reconsideration of the present application as amended.

Claims 1-34 are pending in the present application.

Claims 1-7, and 26-32 are rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter.

Claims 1-34 are rejected under 35 U.S.C. §102(a) as being unpatentable over a publication entitled "Timing Optimization of FPGA Placements by Logic Replication", Design Automation Conference, 2003 Proceedings ("Beraudo").

Claims 1-34 are rejected under 35 U.S.C. §102(a) as being unpatentable over a publication entitled "Temporal Logic Replication for Dynamically Reconfigurable FPGA Partitioning", IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems ("Mak").

Claims 1-34 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 6,099,583 ("Nag").

Claims 1, 8, 14, 21, 26, and 33 have been amended.

Claims 35 and 36 have been added.

Support for amended claims 1, 8, 14, 21, 26, and 33 is found on pages 11-15 and 23 in the specification, Figures 1 and 4 in the drawings, and in claims 1-34 as originally filed. Applicants submit that no new matter has been added.

Claims 1-7, and 26-32 are rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. Specifically, the Office Action mailed 10/6/2006 states

> The above claims do not return a tangible result, but instead conclude on a step identifying components which in and of itself is likened to a thought that has not been conveyed. Some sort of conveyance of the identification must be made (saving, showing, using) to indicate a tangible result to the process.

(10/6/2006 Office Action, p 2).

Claims 1 and 26 have been amended to further include the limitations of "duplicating the components to replicate; and determining placement locations for duplicates of the components to replicate to be placed with the components to replicate on the target device". Applicants submit that claims 1 and 26, as amended, produce a tangible result.

In view of the amendments made to claims 1 and 26, Applicants submit that the rejection to claims 1-7 and 26-32 under 35 U.S.C. §101 have been overcome.

Claims 1-34 are rejected under 35 U.S.C. §102(a) as being unpatentable over Beraudo.

Claims 1-34 are also rejected under 35 U.S.C. §102(a) as being unpatentable over Mak.

Applicants submit that the subject matter of claims 1-34 in the present application were invented prior to June 2, 2003 and July 2003 the publication dates of Beraudo and Mak as listed on form PTO-892 issued by the Patent Office . Applicants have submitted herewith a declaration of prior invention by the inventors under 37 C.F.R. §1.131. Applicants submit that the rejection to claims 1-34 have been overcome.

Claims 1-34 are rejected under 35 U.S.C. §102(e) as being unpatentable over Nag. Specifically, the Office Action mailed 10/6/2006 states in part that

> Claims 1-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Nag, U.S. Patent No. 6,099,583. Nag teaches a method of incrementally improving the placement of a FPGA design by moving logic components according to a annealing process that includes a incremental movement according to a cost function based upon slack value (Figure 24, column 25 line 62 – column 26 line 20, column 40 lines 42-63,). As exemplified in Figure 24, Nag removes the logic from it's current location, performs slack allocation, and then places duplicate logic in a new location.

(10/6/2006 Office Action, p. 4).

Nag includes a disclosure of a core-based PLD programming method for programming a PLD to implement a user-defined logic operation including a set of cores. The PLD includes several configurable logic blocks (CLBs). Each core includes several logic portions that are arranged in a fixed pattern, and each logic portion includes configuration data for configuring one CLB. A placement process is performed during which only a single reference logic portion of each core is placed in a configuration

data table to form a first placement pattern. Non-reference portions of the cores are not placed in the configuration data table during the initial placement process. An annealing process is then performed during which the reference logic portions associated with the cores are moved between CLB sites in an attempt to identify an optimal placement solution. A separate CLB site overlap table is utilized to keep track of the non-reference logic portions during the annealing process. The CLB site overlap table includes memory locations that are assigned to each CLB site. Each memory location stores an integer value indicating the number of reference logic portions and non-reference logic portions assigned to an associated CLB site. A cost value that is based on the placement arrangement and overlap information is utilized by an annealing engine to "drive" the annealing process toward an optimal placement solution. After an optimal placement solution is found, the non-reference logic portions of the cores are placed (Nag Abstract).

Applicants submit that Nag does not teach or suggest synthesizing a design for a system, mapping components in the design onto resources on a target device, determining placement locations for the components on the target device, identifying components to replicate in response to criticality determined from the placement locations, duplicating the components to replicate, and determining placement locations for duplicates of the components to replicate to be placed on the target device together with the components to replicate.

On the contrary, Nag discloses a post-annealing residual overlap removal process that includes "temporarily removing individual logic portions" 2410. The "individual logic portions removed in Step 2410 are replaced using bipartite matching to complete the revised placement solution" (Nag col. 25, lines 65-67, and col. 26, lines 17-20, and Figure 4, 2410 and 2460). Applicants submit that the individual logic portions are not duplicated and placed together with the original individual logic portions on an FPGA. Figure 22 illustrates logic portions 2210, 2220, and 2230 as placed (Nag col. 24, lines 49-54 and Figure 22). Figure 25 illustrates logic portions 2210, 2220, and 2230 as removed from CLB sites CLB (1,4), CLB (9,1), and CLB(10,3) in accordance with Step 2410 (Nag col. 26, lines 24-29 and Figure 25). Figure 54 illustrates the replacement of individual logic portions 2210, 2220, and 2230 in accordance

with Step 2460 (Nag col. 40, lines 42-46 and Figure 54). Logic portions 2210, 2220, and 2230 are simply moved (removed Step 2410 and replaced Step 2460). As shown in Figure 54, only a single copy of logic portions 2210, 2220, and 2230 reside on the FPGA. Clearly, Nag does not duplicate components to replicate, and determine placement locations for duplicates of the components to replicate to be placed on a target device together with the components to replicate.

In contrast, claim 1 states

> A method for designing a system on a target device utilizing field programmable gate arrays (FPGAs), comprising:
> synthesizing a design for the system;
> mapping components in the design onto resources on the target device;
> determining placement locations for the components on the target device;
> identifying components to replicate in response to criticality determined from the placement locations;
> duplicating the components to replicate; and
> determining placement locations for duplicates of the components to replicate to be placed on the target device together with the components to replicate.

(Claim 1) (Emphasis Added).

Claims 14, and 26 include similar limitations. Given that claims 2-13, and 35 depend from claim 1, claims 15-25 depend from claim 14, and claims 26-34, and 36 depend from claim 26, it is likewise submitted that claims 2-13, 15-25, and 26-36 are also patentable under 35 U.S.C. §102(e).

Applicants submit that Nag also does not teach or suggest identifying components to replicate by identifying a replication candidate with associated slack that exceeds a threshold value.

On the contrary, Nag removes individual logic portions at Step 2410 in order to free the CLB sites for use in the residual overlap removal process (Nag col. 26, lines 26-33 and Figure 25). The individual logic portions 2210, 2220, and 2230 are not removed because they have slack that exceed a threshold value. Furthermore, a slack allocation process at Step 2450 is performed only to determine whether a placement solution for individual logic portions, which have already been identified and removed at step 2410, is optimal (Nag col. 26, lines 12-17 and Figure 25).

In contrast, claim 2 states

> The method of Claim 1, wherein identifying components to replicate comprises identifying a replication candidate with associated slack that exceeds a threshold value.

(Claim 2) (Emphasis Added).

Claims 15 and 27 include similar limitations. Given that claims 3-7, 16-20, 28-32 are dependent on claims 2, 15, and 27, respectively, it is likewise submitted that claims 3-7, 16-20, and 28-32 are also patentable under 35 U.S.C. §102(e).

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-34 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicant's attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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